

What is claimed is:

1. A semiconductor device, comprising:
a semiconductor layer which includes a first semiconductor region of a first conductivity type, a base region of a second conductivity type, and a plurality of second semiconductor regions of the first conductivity type;
a gate wiring which is formed on the semiconductor layer via a first insulating film;
a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions and which are insulated from the gate wiring, wherein the gate wiring is arranged between the main electrodes and upper surfaces of the main electrodes are higher than an upper surface of the uppermost layer of the gate wiring; and
a connecting plate which is directly connected onto uppermost layers of the main electrodes.
2. The semiconductor device according to claim 1, wherein the uppermost layers of the plurality of main electrodes are a metal layer common to the plurality of main electrodes.
3. The semiconductor device according to claim 2, further comprising a second insulating film which is formed on the surface of the uppermost layer of the gate wiring.
4. The semiconductor device according to claim 1, wherein the main electrodes are formed of a plurality of metal layers, and a second insulating film extends between the plurality of metal layers.
5. The semiconductor device according to claim 1, wherein the plurality of main electrodes are formed apart from the gate wiring with a gap therebetween.
6. A semiconductor device, comprising:
a semiconductor layer which includes a first semiconductor

region of a first conductivity type, a base region of a second conductivity type, and a cell forming region in which a plurality of second semiconductor regions of the first conductivity type are formed;

a first gate electrode which is formed in the cell forming region and controls continuity/non-continuity between the first semiconductor region and the second semiconductor region;

a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions respectively and which are formed at predetermined intervals in the cell forming region on the semiconductor layer;

a gate wiring which is formed on the semiconductor layer between the plurality of main electrodes via a first insulating film and which leads out the first gate electrode to an outer peripheral region of the cell forming region, wherein upper surfaces of the uppermost layers of the plurality of main electrodes are higher than an upper surface of the uppermost layer of the gate wiring; and

a first connecting plate which is directly connected onto the plurality of main electrodes.

7. The semiconductor device according to claim 6, wherein the uppermost layers of the plurality of main electrodes are a metal layer common to the plurality of main electrodes.

8. The semiconductor device according to claim 7, further comprising a second insulating film which is formed on the surface of the uppermost layer of the gate wiring.

9. The semiconductor device according to claim 8, wherein the plurality of main electrodes comprise a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

wherein the second main electrode layer is formed on the second insulating film.

10. The semiconductor device according to claim 6,

wherein the gate wiring extends to the outer peripheral region of the cell forming region, and

the semiconductor device further comprises a second gate electrode which is formed on the gate wiring extending to the outer peripheral region of the cell forming region.

11. The semiconductor device according to claim 10, wherein the second gate electrode extends to the cell forming region.

12. The semiconductor device according to claim 11, further comprising a third insulating film which is formed on the surface of the gate wiring extending to the outer peripheral region,

wherein the third insulating film extends to the cell forming region, and the second gate electrode is formed on the third insulating film in the cell forming region.

13. The semiconductor device according to claim 12, wherein the main electrode comprises a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

the third insulating film extends onto the first main electrode layer.

14. The semiconductor device according to claim 10, wherein the second gate electrode is formed of the same material as the uppermost layer of the main electrode.

15. The semiconductor device according to claim 10, wherein the outer peripheral region of the cell forming region is formed at the outer periphery of a semiconductor chip.

16. The semiconductor device according to claim 15, wherein the second gate electrode is formed at the corner of the outer periphery of the semiconductor chip.

17. The semiconductor device according to claim 6, wherein the plurality of main electrodes are formed apart from the gate wiring

with a gap therebetween.

18. The semiconductor device according to claim 10, further comprising a second connecting plate which is directly connected to an upper surface of the second gate electrode, wherein a lead frame is connected to the second connecting plate.

19. The semiconductor device according to claim 6, wherein the gate wiring comprises a first metal layer which is formed on the semiconductor layer and a second metal layer which is formed on the first metal layer.

20. The semiconductor device according to claim 19, wherein the second metal layer contains aluminum (Al).

21. The semiconductor device according to claim 6, wherein the uppermost layers of the plurality of main electrodes and the first connecting plate contain aluminum (Al).

22. The semiconductor device according to claim 6, wherein the first connecting plate is connected to a lead frame.

23. The semiconductor device according to claim 6, wherein the first connecting plate is connected to the plurality of main electrodes by ultrasonic bonding.

24. A semiconductor device, comprising:
a first semiconductor layer of a first conductivity type;
a second semiconductor layer of a second conductivity type which is formed on the first semiconductor layer;
a first semiconductor region of the first conductivity type which is formed in a first cell forming region in the second semiconductor layer;
a second semiconductor region of the first conductivity type which is formed in a second cell forming region in the second semiconductor layer;
a first gate electrode which is formed in the first cell

forming region and controls continuity/non-continuity between the first semiconductor region and the first semiconductor layer;

a second gate electrode which is formed in the second cell forming region and controls continuity/non-continuity between the second semiconductor region and the first semiconductor layer;

a first main electrode which is electrically connected to the first semiconductor region and formed in the first cell forming region on the second semiconductor layer;

a second main electrode which is electrically connected to the second semiconductor region and formed in the second cell forming region on the second semiconductor layer;

a gate wiring which is formed on the second semiconductor layer between the first main electrode and the second main electrode via a first insulating film and which leads out the first and second gate electrodes to an outer peripheral region of the first and second cell forming regions, wherein an upper surface of the uppermost layer of the first main electrode and an upper surface of the uppermost layer of the second main electrode are higher than an upper surface of the uppermost layer of the gate wiring; and

a first connecting plate which is directly connected onto the first main electrode and the second main electrode.

25. The semiconductor device according to claim 24, wherein the uppermost surface of the first main electrode and the uppermost surface of the second main electrode are a common metal layer.

26. The semiconductor device according to claim 25, further comprising a second insulating film which is formed on the surface of the uppermost layer of the gate wiring.

27. The semiconductor device according to claim 26, wherein the first main electrode comprises a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and

wherein the second main electrode layer is formed on the second insulating film.

28. The semiconductor device according to claim 25, wherein the gate wiring extends to the outer peripheral region of the first and second cell forming regions, and the semiconductor device further comprises a third gate electrode which is formed on the gate wiring extending to the outer peripheral region of the first and second cell forming regions.

29. The semiconductor device according to claim 28, wherein the third gate electrode extends to the first or second cell forming region.

30. The semiconductor device according to claim 29, further comprising a third insulating film which is formed on the surface of the gate wiring extending to the outer peripheral region, wherein the third insulating film extends to the first or second cell forming region, and the third gate electrode is formed on the third insulating film in the first or second cell forming region.

31. The semiconductor device according to claim 30, wherein the first main electrode comprises a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, and wherein the third insulating film extends onto the first main electrode layer.

32. The semiconductor device according to claim 28, wherein the third gate electrode is formed of the same material as the uppermost layer of the first main electrode.

33. The semiconductor device according to claim 28, wherein the outer peripheral region of the first and the second cell forming region is formed at the outer periphery of a semiconductor chip.

34. The semiconductor device according to claim 33, wherein

the third gate electrode is formed at the corner of the outer periphery of the semiconductor chip.

35. The semiconductor device according to claim 25, wherein the first main electrode and the second main electrode are formed apart from the gate wiring with a gap therebetween.

36. The semiconductor device according to claim 28, further comprising a second connecting plate which is directly connected to an upper surface of the third gate electrode, wherein a lead frame is connected to the second connecting plate.

37. The semiconductor device according to claim 24, wherein the gate wiring comprises a first metal layer which is formed on the second semiconductor layer and a second metal layer which is formed on the first metal layer.

38. The semiconductor device according to claim 37, wherein the second metal layer contains aluminum (Al).

39. The semiconductor device according to claim 24, wherein the uppermost layer of the first main electrode, the uppermost layer of the second main electrode, and the first connecting plate contain aluminum (Al).

40. The semiconductor device according to claim 24, wherein the first connecting plate is connected to a lead frame.

41. The semiconductor device according to claim 24, wherein the first connecting plate is connected to the first main electrode and the second main electrode by ultrasonic bonding.